

PATENT ABSTRACTS OF JAPAN

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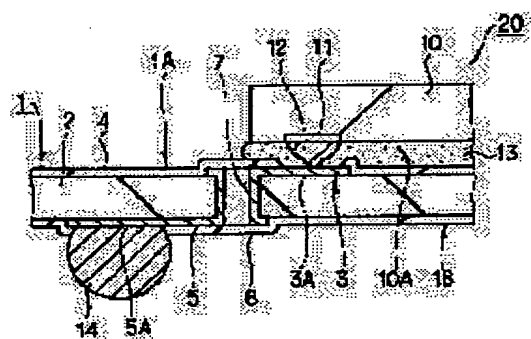
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(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To elongate the lifetime of connections between electrode pads of a wiring substrate and electrode pads of a semiconductor chip by constituting the wiring substrate having electrode pads of a second group electrically connected to electrode pads of a first group with a main substrate material of a flexible film.

SOLUTION: A wiring substrate 1 has a squared planar shape, and is mainly constituted by a flexible film 2 of polyimide-family insulator resin. A plurality of wires 3 are formed on a main surface 1A of the wiring substrate 1, and for the wires 3, electrode pads 3A of a first group are respectively formed. Also, a plurality of wires 5 are formed on the other main surface 1B of the wiring substrate 1, and for the wires 5, electrode pads 5A of a second group are respectively formed. With such arrangements, a semiconductor chip 10 is mounted on the main surface 1A side of the wiring substrate 1, and a plurality of conductive bumps 14 are arranged as external terminals on the other main surface 1B side of the wiring substrate 1.



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CLAIMS

[Claim(s)]

[Claim 1] The 1st principal plane and the 2nd principal plane which counter mutually, and the 1st electrode pad formed in said 1st principal plane, The wiring substrate which has the 2nd electrode pad which was formed in said 2nd principal plane and connected to said 1st electrode pad and electric target, The semiconductor chip which has the 3rd electrode pad formed in the 3rd principal plane and this 3rd principal plane, With the 1st bump who intervened between the 1st electrode pad of said wiring substrate, and the 3rd electrode pad of said semiconductor chip It is the semiconductor device which has the resin which intervened between the 1st principal plane of said wiring substrate, and the 3rd principal plane of said semiconductor chip, and the 2nd bump formed on the 2nd electrode pad of said wiring substrate, and is characterized by said wiring substrate having composition which makes a subject the base material which consists of a flexible film.

[Claim 2] It is the semiconductor device characterized by for said resin being different direction conductive resin with which many conductive particles were mixed into insulating resin in a semiconductor device according to claim 1, for said semiconductor chip intervening said resin and adhesion immobilization being carried out at said wiring substrate.

[Claim 3] It is the semiconductor device characterized by said 1st bump having fixed in a semiconductor device according to claim 2 to the 1st electrode pad of said wiring substrate, or the 3rd electrode pad of said semiconductor chip.

[Claim 4] It is the semiconductor device characterized by said 1st bump having fixed in a semiconductor device according to claim 1 to the 1st electrode pad of said wiring substrate, and the 3rd electrode pad of said semiconductor chip.

[Claim 5] The 1st principal plane and the 2nd principal plane which counter mutually, and the 1st electrode pad formed in said 2nd principal plane, The wiring substrate which has the 2nd electrode pad which was formed in said 2nd principal plane and connected to said 1st electrode pad and electric target, The semiconductor chip which has the 3rd electrode pad formed in the 3rd principal plane and this 3rd principal plane, With the 1st bump who intervened between the 1st electrode pad of said wiring substrate, and the 3rd electrode pad of said semiconductor chip The semiconductor device characterized by having the resin which intervened between the 2nd principal plane of said wiring substrate, and the 3rd principal plane of said semiconductor chip, and the 2nd bump formed on the 2nd electrode pad of said wiring substrate.

[Claim 6] It is the semiconductor device characterized by projecting rather than the 4th principal plane which said 2nd bump counters with the 3rd principal plane of said semiconductor chip in a semiconductor device according to claim 5.

[Claim 7] It is the semiconductor device characterized by for said resin being different direction conductive resin with which many conductive particles were mixed into insulating resin in a semiconductor device according to claim 6, for said semiconductor chip intervening said resin and adhesion immobilization being carried out at said wiring substrate.

[Claim 8] It is the semiconductor device characterized by said 1st bump having fixed in a semiconductor device according to claim 7 to the 1st electrode pad of said wiring substrate, or the 3rd electrode pad of said semiconductor chip.

[Claim 9] It is the semiconductor device characterized by said 1st bump having fixed in a semiconductor device according to claim 6 to the 1st electrode pad of said wiring substrate, and the 3rd electrode pad of said semiconductor chip.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] About a semiconductor device, especially this invention is applied to a BGA mold semiconductor device, and relates to an effective technique.

[0002]

[Description of the Prior Art] As a suitable semiconductor device for the formation of a many-items child, the semiconductor device called a BGA (Ball Grid Array) mold is known. In this BGA mold semiconductor device, the attempt manufactured using different direction conductive resin is made. Manufacture of the BGA mold semiconductor device using different direction conductive resin Although not limited to this, a conductive bump is formed on the electrode pad formed in one principal plane of a semiconductor chip, for example. Then, while intervening different direction conductive resin on the 1 principal plane of a wiring substrate, positioning a semiconductor chip, sticking a semiconductor chip by pressure in the condition of having heated, after that and carrying out adhesion immobilization of the semiconductor chip at a wiring substrate The conductive bump formed on the electrode pad formed in one principal plane of a wiring substrate and the electrode pad of a semiconductor chip is connected electrically. Then, it is carried out by forming the conductive bump used as an external terminal on the electrode pad formed in one principal plane of a wiring substrate, and other principal planes which counter. Thus, since the manufactured BGA mold semiconductor device can distribute the stress resulting from the thermal expansion difference of a wiring substrate and a semiconductor chip with the different direction conductive resin which intervened between the wiring substrate and the semiconductor chip, its connection life of the connection between the electrode pad of a wiring substrate and the electrode pad of a semiconductor chip is long.

[0003] In addition, the technique of mounting a semiconductor chip using different direction conductive resin is indicated by the JP,8-37208,A (February 6, 1996 disclosure) official report and the list at the JP,8-236578,A (September 13, 1996 disclosure) official report, for example. Moreover, the BGA mold semiconductor device using different direction conductive resin is indicated by the JP,10-270496,A (October 9, 1998 disclosure) official report, for example.

[0004]

[Problem(s) to be Solved by the Invention] this invention person etc. found out the following troubles, as a result of examining the BGA mold semiconductor device which used different direction conductive resin.

[0005] (1) If stress other than the stress resulting from the thermal expansion difference of a wiring substrate and a semiconductor chip is added, the stress concerning the different direction conductive resin which intervened between the wiring substrate and the semiconductor chip will increase, and the connection life of the connection between the electrode pad of a wiring substrate and the electrode pad of a semiconductor chip will become short.

[0006] Since the stress concerning different direction conductive resin increases from the difference in the thermal expansion difference of a mounting substrate and a wiring substrate, the difference in the thermal expansion difference of a mounting substrate and a semiconductor chip, etc. when a BGA mold semiconductor device is mounted in a mounting substrate, the connection life of the connection between the electrode pad of a wiring substrate and the electrode pad of a semiconductor chip becomes short. That is, the connection life of a connection becomes [the direction after mounting rather than the condition before mounting] short. In the BGA mold semiconductor device which has stationed the conductive bump as an external terminal especially in addition to the projection field of a semiconductor chip, since the stress which originates in a thermal expansion difference with a mounting substrate, and is applied to different direction conductive resin is large, the connection life of a connection becomes short.

[0007] Therefore, it is necessary to make it not, tell the effect of a mounting substrate to different direction conductive resin if possible in a BGA mold semiconductor device.

[0008] (2) Since the BGA mold semiconductor device using different direction conductive resin mounts the semiconductor chip by the face down method on the 1 principal plane of a wiring substrate, it can attain thin shape-ization by the face-up method on the 1 principal plane of a wiring substrate as compared with the BGA mold semiconductor device which mounted the semiconductor chip.

[0009] However, since the BGA mold semiconductor device has the composition that the conductive bump was placed between the 1 principal-plane side of a wiring substrate, the semiconductor chip has been arranged, and the conductive bump as an external terminal has been stationed at the principal plane side of everything but a wiring substrate, it is becoming difficult to attain thin shape-ization further.

[0010] The object of this invention is to offer the technique which can lengthen the connection life of the connection between the electrode pad of a wiring substrate, and the electrode pad of a semiconductor chip.

[0011] Other objects of this invention are to offer the technique which can attain thin shape-ization of a semiconductor device.

[0012] As new along [said] this invention a description as the other objects will become clear by description and the accompanying drawing of this description.

[0013]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0014] (1) The 1st principal plane and the 2nd principal plane which counter mutually, and the 1st electrode pad formed in said 1st principal plane, The wiring substrate which has the 2nd electrode pad which was formed in said 2nd principal plane and connected to said 1st electrode pad and electric target, The semiconductor chip which has the 3rd electrode pad formed in the 3rd principal plane and this 3rd principal plane, With the 1st bump who intervened between the 1st electrode pad of said wiring substrate, and the 3rd electrode pad of said semiconductor chip It is the semiconductor device which has the resin which intervened between the 1st principal plane of said wiring substrate, and the 3rd principal plane of said semiconductor chip, and the 2nd bump formed on the 2nd electrode pad of said wiring substrate, and said wiring substrate has composition which makes a subject the base material which consists of a flexible film.

[0015] (2) The 1st principal plane and the 2nd principal plane which a semiconductor device counters mutually, and the 1st electrode pad formed in said 2nd principal plane, The wiring substrate which has the 2nd electrode pad which was formed in said 2nd principal plane and connected to said 1st electrode pad and electric target, The semiconductor chip which has the 3rd electrode pad formed in the 3rd principal plane and this 3rd principal plane, With the 1st bump who intervened between the 1st electrode pad of said wiring substrate, and the 3rd electrode pad of said semiconductor chip It has the composition of having the resin which intervened between the 2nd principal plane of said wiring substrate, and the 3rd principal plane of said semiconductor chip, and the 2nd bump formed on the 2nd electrode pad of said wiring substrate.

[0016] Since according to the above-mentioned means (1) the stress which originates in the thermal expansion difference of a mounting substrate and a wiring substrate, and is applied to resin, and the stress which originates in the thermal expansion difference of a mounting substrate and a semiconductor chip, and is applied to resin can be eased according to deformation of a wiring substrate after mounting a semiconductor device in a mounting substrate, the connection life of the connection between the electrode pad of a wiring substrate and the electrode pad of a semiconductor chip can be lengthened.

[0017] According to the above-mentioned means (2), since the thickness of a semiconductor chip can be offset with the 2nd bump's height, thin shape-ization of a semiconductor device can be attained.

[0018]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. In addition, in the complete diagram for explaining the gestalt of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.

[0019] (Operation gestalt 1) Drawing 1 is the typical sectional view of the BGA mold semiconductor device which is the operation gestalt 1 of this invention, drawing 2 is the typical sectional view which expanded a part of drawing 1, and drawing 3 is a typical sectional view in the condition of having mounted the BGA mold semiconductor device shown in drawing 1 in the mounting substrate. In addition, in order to make a drawing legible, in drawing 1 and drawing 3, a part of hatching of a cross section is omitted.

[0020] As shown in drawing 1 and drawing 2, the BGA mold semiconductor device 20 of this operation gestalt carries one semiconductor chip 10 in the 1 principal-plane 1A side of the wiring substrate 1, and has composition which has stationed two or more conductive bumps 14 as an external terminal to other one principal plane [of the wiring substrate 1], and principal plane (rear face) 1B side which counters. The semiconductor chip 10 is carried as the 1 principal-plane 10A faces one principal plane of the wiring substrate 1.

[0021] The flat-surface configuration of a semiconductor chip 10 is formed by the shape of a rectangle, and is formed with the square of 10[mm] x 10[mm] in this operation gestalt. The logical circuit is built in this semiconductor chip 10 as an integrated circuit.

[0022] The semiconductor chip 10 has the composition of having the surface protective coat (the last protective coat) mainly formed on the 1 principal plane of a semi-conductor substrate and this semi-conductor substrate as covered an insulating layer, the multilayer-interconnection layer which accumulated each of a wiring layer on two or more steps, and this multilayer-interconnection layer. A semi-conductor substrate is formed with single crystal silicon, an insulating layer is formed for example, by the silicon oxide film, and the wiring layer is formed by metal membranes, such as aluminum (aluminum) or an aluminum alloy. Moreover, the surface protective coat is formed with for example, the silicon oxide film or a silicon nitride film. Thus, in the constituted semiconductor chip 10, it has the coefficient of thermal expansion of 3×10^{-6} [1-/degree C] extent.

[0023] Two or more electrode pads (bonding pad) 11 are formed in the periphery of 1 principal-plane (circuit forming face) 10A of a semiconductor chip 10 along each side of the periphery enclosure. Each of two or more electrode pads 11 is formed in the wiring layer of the maximum upper layer of the multilayer-interconnection layers of a semiconductor chip 10. The wiring layer of the maximum upper layer is covered by the surface protective coat formed in that upper layer, and bonding opening which exposes the front face of the electrode pad 11 is formed in

this surface protective coat.

[0024] The flat-surface configuration of the wiring substrate 1 is formed by the shape of a rectangle, and is formed with the square of 25[mm] x25[mm] in this operation gestalt. The wiring substrate 1 has composition which makes a subject the flexible film 2 which consists of insulating resin of a polyimide system as a base material. The flexible film 2 is formed by the thickness of for example, 0.2 [mm] extent.

[0025] As shown in drawing 2, two or more wiring 3 is formed in one principal plane 1A of the wiring substrate 1, and electrode pad 3A is formed in each of these wiring 3 of two or more. Two or more wiring 5 is formed in other principal plane 1B of the wiring substrate 1, and electrode pad 5A is formed in each of these wiring 5 of two or more. Each wiring 3 is electrically connected with each wiring 5 through the through hole wiring 7. Wiring 3 and wiring 5 are formed by etching the metallic foil stuck on the flexible film 2 by intervening in the binder. As a metallic foil, the copper foil of the thickness of 35 [μm] extent is used, for example.

[0026] As wiring 3 is covered to one principal plane 1A of the wiring substrate 1, a protective coat 4 is formed, and opening which exposes the front face of electrode pad 3A is formed in this protective coat 4. As wiring 5 is covered to other principal plane 1B of the wiring substrate 1, a protective coat 6 is formed, and opening which exposes the front face of electrode pad 5A is formed in this protective coat 6. Each of protective coats 4 and 6 is formed by the resin of for example, a polyimide system. Thus, in the constituted wiring substrate 1, it has the coefficient of thermal expansion of 70×10^{-6} [1-/degree C] extent.

[0027] Resin 13 intervenes between 1 principal-plane 1A of the wiring substrate 1, and 1 principal-plane 10A of a semiconductor chip 10, and adhesion immobilization of the semiconductor chip 10 is carried out with resin 13 at the wiring substrate 1. As resin 13, the different direction conductive resin with which many conductive particles (for example, nickel (nickel) particle) were mixed in the thermosetting insulation resin of an epoxy system, for example is used. In such resin 13, it has the coefficient of thermal expansion of 90×10^{-6} [1-/degree C] extent.

[0028] Each of two or more electrode pad 3A formed in 1 principal-plane 1A of the wiring substrate 1 is arranged in each of two or more electrode pads 11 formed in 1 principal-plane 10A of a semiconductor chip 10, and the location which counters. Between the electrode pads 11 of electrode pad 3A of the wiring substrate 1, and semiconductor chip 10A, the conductive bump 12 who consists of gold (Au) intervenes. The conductive bump 12 fixes to the electrode pad 11 of a semiconductor chip 10, and is connected electrically and mechanically. Moreover, the conductive bump 12 intervenes the part of the mixed conductive particles between different direction conductive resin (13), and is electrically connected to it at electrode pad 3A of the wiring substrate 1. Connection with electrode pad 3A of the wiring substrate 1 and the conductive bump 12 is held according to the heat shrink force and heat-curing shrinkage force of resin 13.

[0029] The conductive bump 13 is formed for example, by the ball bonding method. The ball bonding method is the approach of carrying out thermocompression bonding of the ball formed in the point of Au wire to an electrode pad, cutting Au wire from the part of a ball after that, and forming a conductive bump.

[0030] Although each of two or more conductive bumps 14 is not limited to this, it is arranged in the state of the triplex row along each side of the periphery enclosure of the wiring substrate 1 by the periphery except the center section of other principal plane 1B of the wiring substrate 1. Each of two or more conductive bumps 14 fixes to each electrode pad 5A, and is connected electrically and mechanically. The conductive bump 14 is formed by the metal material of a 63[wt%] lead (Pb) -37 [wt%] tin (Sn) presentation for example.

[0031] Next, manufacture of the BGA mold semiconductor device 20 is explained using drawing 1 and drawing 2.

[0032] First, the wiring substrate 1 and a semiconductor chip 10 are prepared. The conductive bump 12 is formed on the electrode pad 11 of a semiconductor chip 10. The conductive bump 12 of this operation gestalt uses Au wire, and is formed by the ball bonding method which used supersonic vibration together to thermocompression bonding. Thus, the formed conductive bump 12 is firmly connected to the electrode pad 11 of a semiconductor chip 10.

[0033] Next, the resin 13 processed in the shape of a film is stuck on the chip loading field of 1 principal-plane 1A of the wiring substrate 1. As resin 13, the different direction conductive resin with which many conductive particles (for example, nickel particle) were mixed in the thermosetting insulation resin of an epoxy system, for example is used.

[0034] Next, resin 13 is intervened on 1 principal-plane 1A of the wiring substrate 1, and a semiconductor chip 10 is arranged. At this time, a semiconductor chip 10 is arranged in the condition that that 1 principal-plane 10A faces 1 principal-plane 1A of the wiring substrate 1. Moreover, a semiconductor chip 10 is arranged as the electrode pad 11 counters with electrode pad 3A of the wiring substrate 1.

[0035] Next, a semiconductor chip 10 is stuck by pressure in the condition of having heated, and resin 13 is stiffened after that. In this process, adhesion immobilization of the semiconductor chip 10 is carried out at the wiring substrate 1 with the resin 13 which intervened between that 1 principal-plane 10A and 1 principal-plane 1A of the wiring substrate 1. Moreover, the conductive bump 12 intervenes the part of the mixed conductive particles between different direction conductive resin (13), and is electrically connected to it at electrode pad 3A of the wiring substrate 1. Connection with electrode pad 3A of the wiring substrate 1 and the conductive bump 12 is held according to the heat shrink force and heat-curing shrinkage force of resin 13.

[0036] Next, the conductive bump 14 is formed on electrode pad 5A of other principal plane 1B of the wiring substrate 1. Although not limited to this, the conductive bump's 14 formation supplies the metal ball which consists of a 63[wt%] lead (Pb) -37 [wt%] tin (Sn) presentation by the ball supplying method on electrode pad 5A of the wiring substrate 1, for example, and is performed by fusing a metal ball after that. Thereby, the BGA mold semiconductor device 20 shown in drawing 1 and drawing 2 is completed mostly.

[0037] Thus, the constituted BGA mold semiconductor device 20 is mounted in a mounting substrate, and is built into electronic equipment, such as Personal Digital Assistant devices, such as a cellular phone, and PDA (Personal Digital Assistants), HPC (Handheld Personal Computer), and a personal computer. As shown in drawing 3, the BGA mold semiconductor device 20 fuses and stiffens the conductive bump 14, and is mounted by connecting the conductive bump 14 to the electrode pad 31 of the mounting substrate 30 electrically and mechanically.

[0038] By the way, the wiring substrate 1 which uses the flexible film 2 as a base material is used for the BGA mold semiconductor device 20 of this operation gestalt. This wiring substrate 1 is soft as compared with the wiring substrate which consists of a hard substrate which carried out impregnation of epoxy system resin or the polyimide system resin to the glass fiber, and since it is easy to deform it, it can ease the stress which originates in the thermal expansion difference of the mounting substrate 30 and a semiconductor chip 10, and is applied to resin 13, and the stress which originates in the thermal expansion difference of the mounting substrate 30 and a semiconductor chip 10, and is applied to resin 13 according to deformation of the wiring substrate 1. It is important to ease such stress according to deformation of the wiring substrate 1 especially, since the stress which originates in the thermal expansion difference of the mounting substrate 30 and a semiconductor chip 10, and is applied to resin 13, and the stress which originates in the thermal expansion difference of the mounting substrate 30 and a semiconductor chip 10, and is applied to resin 13 are large when the conductive bump 14 as an external terminal has been stationed like this operation gestalt in addition to the projection field of a semiconductor chip 10.

[0039] Thus, according to this operation gestalt, the following effectiveness is acquired. In the BGA mold semiconductor device 20, the wiring substrate 1 has composition which makes a subject the base material which consists of a flexible film 2. Thus, after mounting the BGA mold semiconductor device 20 in the mounting substrate 30 by constituting, Since the stress which originates in the thermal expansion difference of the mounting substrate 30 and the wiring substrate 1, and is applied to resin 13, and the stress which originates in the thermal expansion difference of the mounting substrate 30 and a semiconductor chip 10, and is applied to resin 13 can be eased according to deformation of the wiring substrate 1 The connection life of the connection between electrode pad 3A of the wiring substrate 1 and the electrode pad 11 of a semiconductor chip 10 can be lengthened.

[0040] Moreover, since the connection life of the connection between electrode pad 3A of the wiring substrate 1 and the electrode pad 11 of a semiconductor chip 10 can be lengthened, improvement of dependability to mounting of the BGA mold semiconductor device 20 can be aimed at.

[0041] In addition, although this operation gestalt explained the example in which the conductive bump 12 was formed on the electrode pad 11 of a semiconductor chip 10, the conductive bump 12 may form on electrode pad 3A of the wiring substrate 1, as shown in drawing 4 (typical sectional view). Also in this case, the same effectiveness as the above-mentioned operation gestalt 1 is acquired.

[0042] Moreover, although this operation gestalt explained the example which stuck film-like resin 13 on the chip loading field of 1 principal-plane 1A of the wiring substrate 1, liquefied resin 13 may be applied to the chip loading field of 1 principal-plane 1A of the wiring substrate 1.

[0043] Moreover, although this operation gestalt explained the example which used different direction conductive resin as resin 13, the thermosetting resin or thermoplastics with which the conductive particle is not mixed as resin 13 may be used.

[0044] (Operation gestalt 2) Drawing 5 is the typical sectional view showing some BGA mold semiconductor devices which are the operation gestalten 2 of this invention.

[0045] As shown in drawing 5, the BGA mold semiconductor device 21 of this operation gestalt has the same composition as the above-mentioned operation gestalt 1 fundamentally, and the following configurations differ.

[0046] That is, the conductive bump 12 fixes to electrode pad 1A of the wiring substrate 1, and the electrode pad 11 of a semiconductor chip 10, and is connected to these electrode pads electrically and mechanically. The conductive bump 12 is formed by the metal material of the Pb-Sn presentation with the melting point higher than the conductive bump 14 for example. Moreover, resin 13 is formed with the thermosetting resin of for example, an epoxy system.

[0047] Thus, it sets to the constituted BGA mold semiconductor device 21. The conductive bump 12 is fused in the condition of having intervened the conductive bump 12 between electrode pad 3A of the wiring substrate 1, and the electrode pad 11 of a semiconductor chip 10. Electrode pad 3A of the wiring substrate 1 and the electrode pad 11 of a semiconductor chip 10 are connected electrically and mechanically. Then, it is filled up with liquefied resin 13 between 1 principal-plane 1A of the wiring substrate 1, and 1 principal-plane 10A of a semiconductor chip 10, and is manufactured by performing heat treatment and stiffening resin 13 after that.

[0048] Thus, also in the constituted BGA mold semiconductor device 21, the same effectiveness as the above-mentioned operation gestalt 1 is acquired.

[0049] (Operation gestalt 3) Drawing 6 is the typical sectional view of the BGA mold semiconductor device which is the operation gestalt 3 of this invention, drawing 7 is the typical sectional view which expanded a part of drawing 6, and drawing 8 is a typical sectional view in the condition of having mounted the BGA mold semiconductor device shown in drawing 6 in the mounting substrate. In addition, in order to make a drawing legible, in drawing 6 and drawing 8, a part of hatching of a cross section is omitted.

[0050] As shown in drawing 6 and drawing 7, the BGA mold semiconductor device 22 of this operation gestalt has the same composition as the above-mentioned operation gestalt 1 fundamentally, and the following configurations differ.

[0051] That is, the semiconductor chip 10 is carried in other principal plane (rear face) 1B side of the wiring

substrate 1. Moreover, the wiring 5 formed in other principal plane 1B of the wiring substrate 1 has the composition of having electrode pad 5A and electrode pad 3A. Moreover, the conductive bump 14 is formed in the height in which the topmost part 14A projects rather than 1 principal-plane 10A of a semiconductor chip 10, and other principal plane (rear face) 10B to counter.

[0052] Thus, also in the constituted BGA mold semiconductor device 22, the same effectiveness as the above-mentioned operation gestalt 1 is acquired.

[0053] Moreover, in the BGA mold semiconductor device 22, the semiconductor chip 10 is carried in other principal plane 1B side of the wiring substrate 1. Thus, since the thickness of a semiconductor chip 10 can be offset with the conductive bump's 14 height by constituting, thin shape-ization of the BGA mold semiconductor device 22 can be attained.

[0054] Moreover, since it is not necessary to form wiring and a protective coat in 1 principal-plane 1A of the wiring substrate 1, and to form through hole wiring further, low cost-ization of the wiring substrate 1 can be attained.

[0055] Moreover, since other principal plane 10B of a semiconductor chip 10 can be contacted to the mounting substrate 30 in case the BGA mold semiconductor device 22 is mounted in the mounting substrate 30 as shown in drawing 8, the heat of a semiconductor chip 10 of operation can be made to transmit to the mounting substrate 30 from other principal plane 10B of a semiconductor chip 10. Consequently, the heat dissipation effectiveness of the BGA mold semiconductor device 22 improves.

[0056] As mentioned above, although invention made by this invention person was concretely explained based on said operation gestalt, as for this invention, it is needless to say for it to be able to change variously in the range which is not limited to said operation gestalt and does not deviate from the summary.

[0057]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.

[0058] (1) It can set to a semiconductor device and the connection life of the connection between the electrode pad of a wiring substrate and the electrode pad of a semiconductor chip can be lengthened.

[0059] (2) Thin shape-ization of a semiconductor device can be attained.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the typical sectional view of the BGA mold semiconductor device which is the operation gestalt 1 of this invention.

[Drawing 2] It is the typical sectional view which expanded a part of drawing 1 .

[Drawing 3] It is a typical sectional view in the condition of having mounted the BGA mold semiconductor device shown in drawing 1 in the mounting substrate.

[Drawing 4] It is the typical sectional view showing some BGA mold semiconductor devices which are the modifications of the operation gestalt 1 of this invention.

[Drawing 5] It is the typical sectional view showing some BGA mold semiconductor devices which are the operation gestalten 2 of this invention.

[Drawing 6] It is the typical sectional view of the BGA mold semiconductor device which is the operation gestalt 3 of this invention.

[Drawing 7] It is the typical sectional view which expanded a part of drawing 6 .

[Drawing 8] It is a typical sectional view in the condition of having mounted the BGA mold semiconductor device shown in drawing 6 in the mounting substrate.

[Description of Notations]

1 [— Wiring, 3A 5A / — 4 An electrode pad 6 / — A protective coat, 7 / — Through hole wiring, 10 / — A semiconductor chip, 11 / — 12 An electrode pad 14 / — A conductive bump, 13 / — Resin, 20 21 22 / — A semiconductor device, 30 / — A mounting substrate, 31 / — Electrode pad.] — A wiring substrate, 1A — One principal plane, a principal plane besides 1B—, 2 — 3 A flexible film, 5

[Translation done.]

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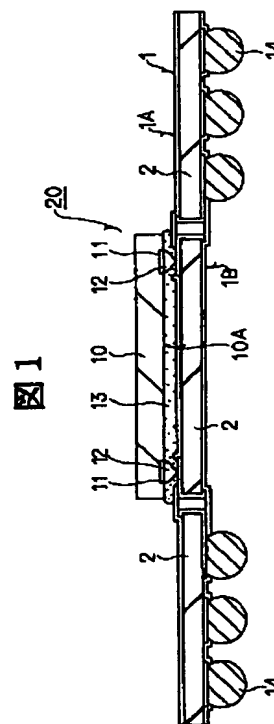
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(54)【発明の名称】 半導体装置

(57)【要約】

【課題】 配線基板の電極パッドと半導体チップの電極パッドとの間における接続部の接続寿命を長くする。

【解決手段】 互いに対向する第1主面及び第2主面と、前記第1主面に形成された第1電極パッドと、前記第2主面に形成され、前記第1電極パッドと電気的に接続された第2電極パッドとを有する配線基板と、第3主面及びこの第3主面に形成された第3電極パッドを有する半導体チップと、前記配線基板の第1電極パッドと前記半導体チップの第3電極パッドとの間に介在された第1バンプと、前記配線基板の第1主面と前記半導体チップの第3主面との間に介在された樹脂と、前記配線基板の第2電極パッド上に形成された第2バンプとを有する半導体装置であって、前記配線基板は、可撓性フィルムからなる基材を主体とする構成になっている。



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【特許請求の範囲】

【請求項1】 互いに対向する第1主面及び第2主面と、前記第1主面に形成された第1電極パッドと、前記第2主面に形成され、前記第1電極パッドと電氣的に接続された第2電極パッドとを有する配線基板と、第3主面及びこの第3主面に形成された第3電極パッドを有する半導体チップと、

前記配線基板の第1電極パッドと前記半導体チップの第3電極パッドとの間に介在された第1バンブと、前記配線基板の第1主面と前記半導体チップの第3主面との間に介在された樹脂と、前記配線基板の第2電極パッド上に形成された第2バンブとを有し、

前記配線基板は、可撓性フィルムからなる基材を主体とする構成になっていることを特徴とする半導体装置。

【請求項2】 請求項1に記載の半導体装置において、前記樹脂は、絶縁性樹脂の中に多数の導電性粒子が混入された異方導電性樹脂であり、前記半導体チップは、前記樹脂を介在して前記配線基板に接着固定されていることを特徴とする半導体装置。

【請求項3】 請求項2に記載の半導体装置において、前記第1バンブは、前記配線基板の第1電極パッド、又は前記半導体チップの第3電極パッドに固着されていることを特徴とする半導体装置。

【請求項4】 請求項1に記載の半導体装置において、前記第1バンブは、前記配線基板の第1電極パッド及び前記半導体チップの第3電極パッドに固着されていることを特徴とする半導体装置。

【請求項5】 互いに対向する第1主面及び第2主面と、前記第2主面に形成された第1電極パッドと、前記第2主面に形成され、前記第1電極パッドと電氣的に接続された第2電極パッドとを有する配線基板と、第3主面及びこの第3主面に形成された第3電極パッドを有する半導体チップと、前記配線基板の第1電極パッドと前記半導体チップの第3電極パッドとの間に介在された第1バンブと、前記配線基板の第2主面と前記半導体チップの第3主面との間に介在された樹脂と、前記配線基板の第2電極パッド上に形成された第2バンブとを有することを特徴とする半導体装置。

【請求項6】 請求項5に記載の半導体装置において、前記第2バンブは、前記半導体チップの第3主面と対向する第4主面よりも突出していることを特徴とする半導体装置。

【請求項7】 請求項6に記載の半導体装置において、前記樹脂は、絶縁性樹脂の中に多数の導電性粒子が混入された異方導電性樹脂であり、前記半導体チップは、前記樹脂を介在して前記配線基板に接着固定されていることを特徴とする半導体装置。

【請求項8】 請求項7に記載の半導体装置において、

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前記第1バンブは、前記配線基板の第1電極パッド、又は前記半導体チップの第3電極パッドに固着されていることを特徴とする半導体装置。

【請求項9】 請求項6に記載の半導体装置において、前記第1バンブは、前記配線基板の第1電極パッド及び前記半導体チップの第3電極パッドに固着されていることを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置に関し、特に、BGA型半導体装置に適用して有効な技術に関するものである。

【0002】

【従来の技術】多端子化に好適な半導体装置として、例えばBGA (Ball Grid Array) 型と呼称される半導体装置が知られている。このBGA型半導体装置においては、異方導電性樹脂を用いて製造する試みがなされている。異方導電性樹脂を用いたBGA型半導体装置の製造は、これに限定されないが、例えば、半導体チップの一面に形成された電極パッド上に導電性バンブを形成し、その後、配線基板の一主面上に異方導電性樹脂を介在して半導体チップを位置決めし、その後、加熱した状態で半導体チップを圧着して、配線基板に半導体チップを接着固定すると共に、配線基板の一主面に形成された電極パッドと半導体チップの電極パッド上に形成された導電性バンブとを電氣的に接続し、その後、配線基板の一主面と対向する他の主面に形成された電極パッド上に外部端子として用いられる導電性バンブを形成することによって行われる。このようにして製造されたBGA型半導体装置は、配線基板と半導体チップとの熱膨張量差に起因する応力を配線基板と半導体チップとの間に介在された異方導電性樹脂によって分散することができるので、配線基板の電極パッドと半導体チップの電極パッドとの間における接続部の接続寿命が長い。

【0003】なお、異方導電性樹脂を用いて半導体チップを実装する技術については、例えば、特開平8-37208号(1996年2月6日公開)公報、並びに特開平8-236578号(1996年9月13日公開)公報に記載されている。また、異方導電性樹脂を用いたBGA型半導体装置については、例えば、特開平10-270496号(1998年10月9日公開)公報に記載されている。

【0004】

【発明が解決しようとする課題】本発明者等は、異方導電性樹脂を用いたBGA型半導体装置について検討した結果、以下の問題点を見出した。

【0005】(1)配線基板と半導体チップとの熱膨張量差に起因する応力以外の応力が加わると、配線基板と半導体チップとの間に介在された異方導電性樹脂にかかる応力が増加し、配線基板の電極パッドと半導体チップ

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の電極パッドとの間における接続部の接続寿命が短くなる。

【0006】実装基板にBGA型半導体装置を実装した場合、実装基板と配線基板との熱膨張量差の違いや、実装基板と半導体チップとの熱膨張量差の違いなどから、異方導電性樹脂にかかる応力が増加するため、配線基板の電極パッドと半導体チップの電極パッドとの間における接続部の接続寿命が短くなる。即ち、実装する前の状態よりも実装した後の方が接続部の接続寿命が短くなる。特に、半導体チップの投影領域以外に外部端子としての導電性バンプを配置したBGA型半導体装置においては、実装基板との熱膨張量差に起因して異方導電性樹脂にかかる応力が大きいため、接続部の接続寿命が短くなる。

【0007】従って、BGA型半導体装置においては、実装基板の影響を異方導電性樹脂になるべく伝えないようにする必要がある。

【0008】(2)異方導電性樹脂を用いたBGA型半導体装置は、配線基板の一主面上にフェースダウン方式で半導体チップを実装しているので、配線基板の一主面上にフェースアップ方式で半導体チップを実装したBGA型半導体装置と比較して薄型化を図ることができる。

【0009】しかしながら、BGA型半導体装置は、配線基板の一主面側に導電性バンプを介在して半導体チップが配置され、配線基板の他の主面側に外部端子としての導電性バンプが配置された構成になっているため、更に薄型化を図ることが困難になってきている。

【0010】本発明の目的は、配線基板の電極パッドと半導体チップの電極パッドとの間における接続部の接続寿命を長くすることが可能な技術を提供することにある。

【0011】本発明の他の目的は、半導体装置の薄型化を図ることが可能な技術を提供することにある。

【0012】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述及び添付図面によって明らかになるであろう。

【0013】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、下記のとおりである。

【0014】(1)互いに対向する第1主面及び第2主面と、前記第1主面に形成された第1電極パッドと、前記第2主面に形成され、前記第1電極パッドと電氣的に接続された第2電極パッドとを有する配線基板と、第3主面及びこの第3主面に形成された第3電極パッドを有する半導体チップと、前記配線基板の第1電極パッドと前記半導体チップの第3電極パッドとの間に介在された第1バンプと、前記配線基板の第1主面と前記半導体チップの第3主面との間に介在された樹脂と、前記配線基板の第2電極パッド上に形成された第2バンプとを有す

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る半導体装置であって、前記配線基板は、可撓性フィルムからなる基材を主体とする構成になっている。

【0015】(2)半導体装置は、互いに対向する第1主面及び第2主面と、前記第2主面に形成された第1電極パッドと、前記第2主面に形成され、前記第1電極パッドと電氣的に接続された第2電極パッドとを有する配線基板と、第3主面及びこの第3主面に形成された第3電極パッドを有する半導体チップと、前記配線基板の第1電極パッドと前記半導体チップの第3電極パッドとの間に介在された第1バンプと、前記配線基板の第2主面と前記半導体チップの第3主面との間に介在された樹脂と、前記配線基板の第2電極パッド上に形成された第2バンプとを有する構成になっている。

【0016】前述の手段(1)によれば、実装基板に半導体装置を実装した後、実装基板と配線基板との熱膨張量差に起因して樹脂にかかる応力や、実装基板と半導体チップとの熱膨張量差に起因して樹脂にかかる応力を配線基板の変形によって緩和することができるので、配線基板の電極パッドと半導体チップの電極パッドとの間における接続部の接続寿命を長くすることができる。

【0017】前述の手段(2)によれば、半導体チップの厚さを第2バンプの高さによって相殺することができるので、半導体装置の薄型化を図ることができる。

【0018】

【発明の実施の形態】以下、図面を参照して本発明の実施の形態を詳細に説明する。なお、発明の実施の形態を説明するための全図において、同一機能を有するものは同一符号を付け、その繰り返しの説明は省略する。

【0019】(実施形態1)図1は本発明の実施形態1であるBGA型半導体装置の模式的断面図であり、図2は図1の一部を拡大した模式的断面図であり、図3は図1に示すBGA型半導体装置を実装基板に実装した状態の模式的断面図である。なお、図面を見易くするため、図1及び図3においては、断面のハッチングを一部省略している。

【0020】図1及び図2に示すように、本実施形態のBGA型半導体装置20は、配線基板1の一主面1A側に一つの半導体チップ10を搭載し、配線基板1の一主面と対向する他の主面(裏面)1B側に外部端子としての複数の導電性バンプ14を配置した構成になっている。半導体チップ10は、その一主面10Aが配線基板1の一主面と向かい合うようにして搭載されている。

【0021】半導体チップ10の平面形状は方形で形成され、本実施形態においては例えば10[mm]×10[mm]の正方形で形成されている。この半導体チップ10には、集積回路として例えば論理回路が内蔵されている。

【0022】半導体チップ10は、主に、半導体基板と、この半導体基板の一主面上において絶縁層、配線層の夫々を複数段に積み重ねた多層配線層と、この多層配

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線層を覆うようにして形成された表面保護膜（最終保護膜）とを有する構成になっている。半導体基板は例えば単結晶シリコンで形成され、絶縁層は例えば酸化シリコン膜で形成され、配線層は例えばアルミニウム（Al）又はアルミニウム合金等の金属膜で形成されている。また、表面保護膜は例えば酸化シリコン膜又は窒化シリコン膜で形成されている。このように構成された半導体チップ10においては、 3×10^{-6} [1/°C]程度の熱膨張係数を有する。

【0023】半導体チップ10の一主面（回路形成面）10Aの周辺部には、その外周囲の各辺に沿って複数の電極パッド（ボンディングパッド）11が形成されている。複数の電極パッド11の夫々は、半導体チップ10の多層配線層のうちの最上層の配線層に形成されている。最上層の配線層はその上層に形成された表面保護膜で覆われ、この表面保護膜には電極パッド11の表面を露出するボンディング開口が形成されている。

【0024】配線基板1の平面形状は方形で形成され、本実施形態においては例えば25 [mm] × 25 [mm] の正方形で形成されている。配線基板1は、基材として例えばポリイミド系の絶縁樹脂からなる可撓性フィルム2を主体とする構成になっている。可撓性フィルム2は、例えば0.2 [mm] 程度の厚さで形成されている。

【0025】図2に示すように、配線基板1の一主面1Aには複数の配線3が形成され、この複数の配線3の夫々には電極パッド3Aが形成されている。配線基板1の他の主面1Bには複数の配線5が形成され、この複数の配線5の夫々には電極パッド5Aが形成されている。各配線3はスルーホール配線7を介して各配線5と電気的に接続されている。配線3及び配線5は、可撓性フィルム2に接着材を介して貼り付けられた金属箔をエッチングすることによって形成される。金属箔としては、例えば35 [μm] 程度の厚さの銅箔が用いられている。

【0026】配線基板1の一主面1Aには配線3を覆うようにして保護膜4が形成され、この保護膜4には電極パッド3Aの表面を露出する開口が形成されている。配線基板1の他の主面1Bには配線5を覆うようにして保護膜6が形成され、この保護膜6には電極パッド5Aの表面を露出する開口が形成されている。保護膜4、6の夫々は、例えばポリイミド系の樹脂で形成されている。このように構成された配線基板1においては、 70×10^{-6} [1/°C]程度の熱膨張係数を有する。

【0027】配線基板1の一主面1Aと半導体チップ10の一主面10Aとの間には樹脂13が介在され、半導体チップ10は樹脂13によって配線基板1に接着固定されている。樹脂13としては、例えばエポキシ系の熱硬化性絶縁樹脂に多数の導電性粒子（例えばニッケル（Ni）粒子）が混入された異方導電性樹脂が用いられている。このような樹脂13においては、 90×10^{-6}

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[1/°C]程度の熱膨張係数を有する。

【0028】配線基板1の一主面1Aに形成された複数の電極パッド3Aの夫々は、半導体チップ10の一主面10Aに形成された複数の電極パッド11の夫々と対向する位置に配置されている。配線基板1の電極パッド3Aと半導体チップ10Aの電極パッド11との間には、例えば金（Au）からなる導電性バンプ12が介在されている。導電性バンプ12は、半導体チップ10の電極パッド11に固着され、電気的にかつ機械的に接続されている。また、導電性バンプ12は、異方導電性樹脂（13）に多数混入された導電性粒子のうちの一部を介在して配線基板1の電極パッド3Aに電気的に接続されている。配線基板1の電極パッド3Aと導電性バンプ12との接続は、樹脂13の熱収縮力及び熱硬化収縮力によって保持されている。

【0029】導電性バンプ13は、例えばボール・ボンディング法によって形成されている。ボール・ボンディング法は、Auワイヤの先端部に形成されたボールを電極パッドに熱圧着し、その後、ボールの部分からAuワイヤを切断して導電性バンプを形成する方法である。

【0030】複数の導電性バンプ14の夫々は、これに限定されないが、配線基板1の他の主面1Bの中央部を除いた周辺部に、配線基板1の外周囲の各辺に沿って三列状態で配列されている。複数の導電性バンプ14の夫々は、夫々の電極パッド5Aに固着され、電気的にかつ機械的に接続されている。導電性バンプ14は、例えば63 [wt %] 鉛（Pb）-37 [wt %] 錫（Sn）組成の金属材で形成されている。

【0031】次に、BGA型半導体装置20の製造について、図1及び図2を用いて説明する。

【0032】まず、配線基板1及び半導体チップ10を準備する。半導体チップ10の電極パッド11上には導電性バンプ12が形成されている。本実施形態の導電性バンプ12は、Auワイヤを使用し、熱圧着に超音波振動を併用したボール・ボンディング法で形成される。このようにして形成された導電性バンプ12は、半導体チップ10の電極パッド11に対して強固に接続される。

【0033】次に、配線基板1の一主面1Aのチップ搭載領域に、例えばフィルム状に加工された樹脂13を貼り付ける。樹脂13としては、例えばエポキシ系の熱硬化性絶縁樹脂に多数の導電性粒子（例えばNi粒子）が混入された異方導電性樹脂を用いる。

【0034】次に、配線基板1の一主面1A上に樹脂13を介在して半導体チップ10を配置する。この時、半導体チップ10は、その一主面10Aが配線基板1の一主面1Aと向い合う状態で配置される。また、半導体チップ10は、その電極パッド11が配線基板1の電極パッド3Aと対向するようにして配置される。

【0035】次に、加熱した状態で半導体チップ10を圧着し、その後、樹脂13を硬化させる。この工程にお

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いて、半導体チップ10は、その一主面10Aと配線基板1の一主面1Aとの間に介在された樹脂13によって配線基板1に接着固定される。また、導電性バンプ12は、異方導電性樹脂(13)に多数混入された導電性粒子のうちの一部を介在して配線基板1の電極パッド3Aに電氣的に接続される。配線基板1の電極パッド3Aと導電性バンプ12との接続は、樹脂13の熱収縮力及び熱硬化収縮力によって保持される。

【0036】次に、配線基板1の他の主面1Bの電極パッド5A上に導電性バンプ14を形成する。導電性バンプ14の形成は、これに限定されないが、例えば、63 [wt%] 鉛(Pb) - 37 [wt%] 錫(Sn) 組成からなる金属ボールを配線基板1の電極パッド5A上にボール供給法で供給し、その後、金属ボールを溶融することによって行われる。これにより、図1及び図2に示すBGA型半導体装置20がほぼ完成する。

【0037】このように構成されたBGA型半導体装置20は、実装基板に実装され、携帯電話、PDA (Personal Digital Assistants)、HPC (Handheld Personal Computer) 等の携帯情報端末機器やパーソナル・コンピュータ等の電子機器に組み込まれる。BGA型半導体装置20は、図3に示すように、導電性バンプ14を溶融して硬化させ、実装基板30の電極パッド31に導電性バンプ14を電氣的にかつ機械的に接続することによって実装される。

【0038】ところで、本実施形態のBGA型半導体装置20は、可撓性フィルム2を基材とする配線基板1を用いている。この配線基板1は、ガラス繊維にエポキシ系樹脂又はポリイミド系樹脂を含浸させた硬質基板からなる配線基板と比較して柔らかく、変形し易いため、実装基板30と半導体チップ10との熱膨張量差に起因して樹脂13にかかる応力や、実装基板30と半導体チップ10との熱膨張量差に起因して樹脂13にかかる応力を配線基板1の変形によって緩和することができる。特に、本実施形態のように、半導体チップ10の投影領域以外に外部端子としての導電性バンプ14を配置した場合、実装基板30と半導体チップ10との熱膨張量差に起因して樹脂13にかかる応力や、実装基板30と半導体チップ10との熱膨張量差に起因して樹脂13にかかる応力が大きいため、これらの応力を配線基板1の変形によって緩和することは重要である。

【0039】このように、本実施形態によれば、以下の効果が得られる。BGA型半導体装置20において、配線基板1は、可撓性フィルム2からなる基材を主体とする構成になっている。このように構成することにより、実装基板30にBGA型半導体装置20を実装した後、実装基板30と配線基板1との熱膨張量差に起因して樹脂13にかかる応力や、実装基板30と半導体チップ10との熱膨張量差に起因して樹脂13にかかる応力を配線基板1の変形によって緩和することができるので、配

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線基板1の電極パッド3Aと半導体チップ10の電極パッド11との間における接続部の接続寿命を長くすることができる。

【0040】また、配線基板1の電極パッド3Aと半導体チップ10の電極パッド11との間における接続部の接続寿命を長くすることができるので、BGA型半導体装置20の実装に対する信頼性の向上を図ることができる。

【0041】なお、本実施形態では、半導体チップ10の電極パッド11上に導電性バンプ12を形成した例について説明したが、導電性バンプ12は、図4(模式的断面図)に示すように、配線基板1の電極パッド3A上に形成してもよい。この場合においても、前述の実施形態1と同様の効果が得られる。

【0042】また、本実施形態では、配線基板1の一主面1Aのチップ搭載領域にフィルム状の樹脂13を貼り付けた例について説明したが、配線基板1の一主面1Aのチップ搭載領域に液状の樹脂13を塗布してもよい。

【0043】また、本実施形態では、樹脂13として異方導電性樹脂を用いた例について説明したが、樹脂13としては導電性粒子が混入されていない熱硬化性樹脂又は熱可塑性樹脂を用いてもよい。

【0044】(実施形態2) 図5は本発明の実施形態2であるBGA型半導体装置の一部を示す模式的断面図である。

【0045】図5に示すように、本実施形態のBGA型半導体装置21は、基本的に前述の実施形態1と同様の構成になっており、以下の構成が異なっている。

【0046】即ち、導電性バンプ12は、配線基板1の電極パッド1A及び半導体チップ10の電極パッド11に固着され、これらの電極パッドに電氣的にかつ機械的に接続されている。導電性バンプ12は、導電性バンプ14よりも融点が高い例えばPb-Sn組成の金属材料で形成されている。また、樹脂13は、例えばエポキシ系の熱硬化性樹脂で形成されている。

【0047】このように構成されたBGA型半導体装置21においては、配線基板1の電極パッド3Aと半導体チップ10の電極パッド11との間に導電性バンプ12を介在した状態で導電性バンプ12を溶融して、配線基板1の電極パッド3Aと半導体チップ10の電極パッド11とを電氣的にかつ機械的に接続し、その後、配線基板1の一主面1Aと半導体チップ10の一主面10Aとの間に液状の樹脂13を充填し、その後、熱処理を施して樹脂13を硬化させることによって製造される。

【0048】このように構成されたBGA型半導体装置21においても、前述の実施形態1と同様の効果が得られる。

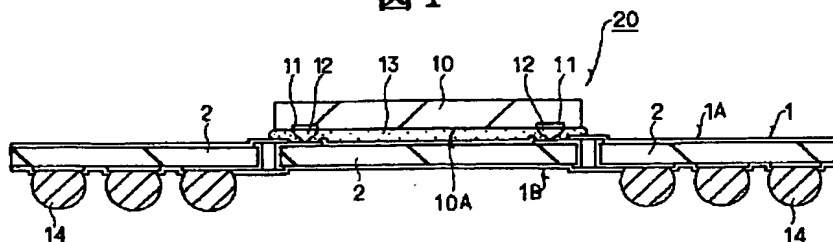
【0049】(実施形態3) 図6は本発明の実施形態3であるBGA型半導体装置の模式的断面図であり、図7は図6の一部を拡大した模式的断面図であり、図8は図

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【0056】以上、本発明者によってなされた発明を、

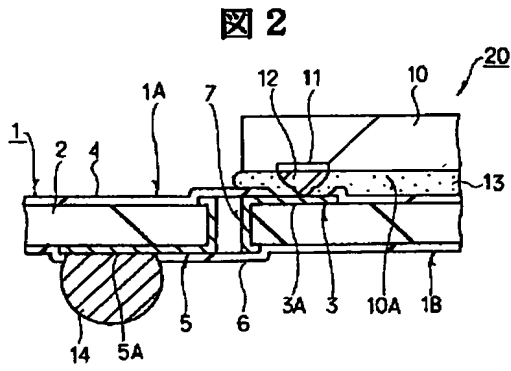
【图 1】

图 1

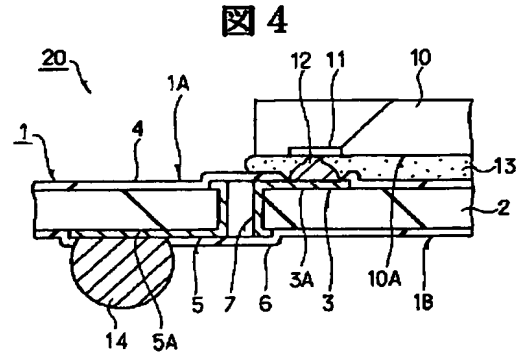


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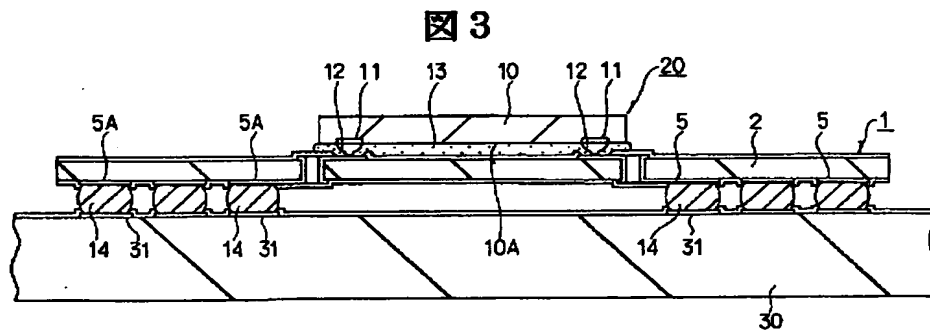
【図2】



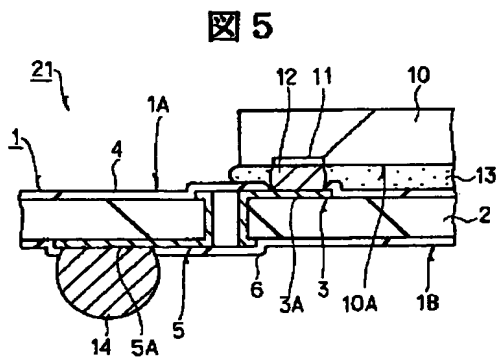
【図4】



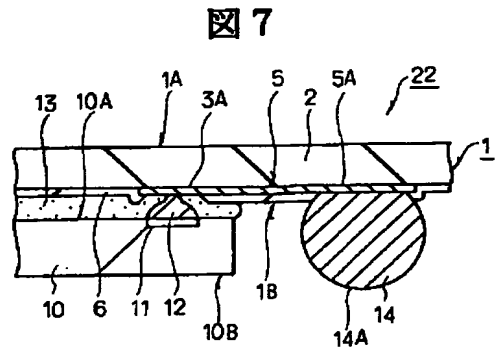
【図3】



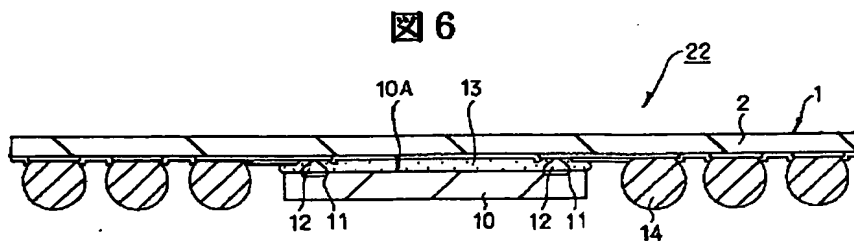
【図5】



【図7】



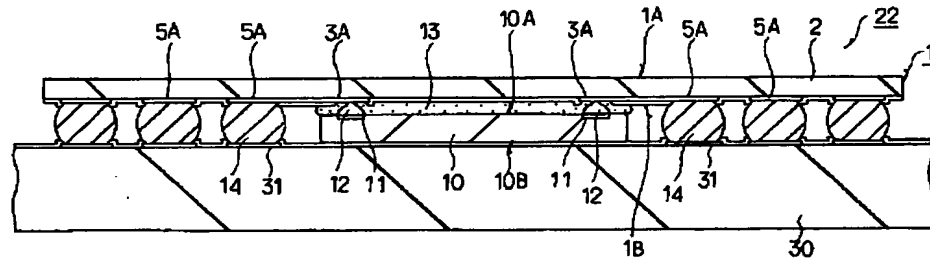
【図6】



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【図8】

図8



フロントページの続き

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